AMENDMENTS TO THE CLAIMS

Please cancel claims 3, 8, 10, 11, 13, 14 and 25 without prejudice.

1. (CURRENTLY AMENDED) An integrated circuit comprising:

a die having a surface;

a first area of first circuit cells in said die configurable by user defined interconnections from above said surface; and

a second area comprising a plurality of sub-circuit cells forming a module ~~having a predefined functionality~~, wherein said sub-circuit cells ~~include at least one second circuit cell configured such that when said predefined functionality of said module is not used, said second circuit cell is configurable by user defined interconnections from above said surface~~ includes (i) one or more non-reusable circuit cells coupled to a custom specific layer in a custom design having a predefined functionality and (ii) one or more reusable circuit cells coupled to said custom specific layer in said custom design when said predefined functionality of said module is not used.

2. (CURRENTLY AMENDED) The integrated circuit of claim 1, wherein said ~~second~~ and of said reusable circuit cell comprises

at least one of a buffer circuit cell, an inverter circuit cell, a flip-flop circuit cell, a latch circuit cell, a multiplexer circuit cell, an exclusive-OR gate circuit cell, an AND gate circuit cell, and an OR gate circuit cell.

3. (CANCEL)

4. (CURRENTLY AMENDED) The integrated circuit of claim ~~3~~1, wherein said ~~plurality of second circuit cells comprises~~ reusable circuit cell comprise a plurality of different circuit cell types.

5. (ORIGINAL) The integrated circuit of claim 1, wherein each of said first circuit cells comprises an input terminal at said surface and an output terminal at said surface.

6. (CURRENTLY AMENDED) The integrated circuit of claim ~~1~~29, wherein said ~~at least one second circuit cell~~ reusable circuit cell comprises a first input terminal ~~at said surface~~ and a first output terminal ~~at said surface~~.

7. (CURRENTLY AMENDED) The integrated circuit of claim 6, ~~further comprising:~~

~~at least one layer of conductive interconnections formed on said surface,~~

wherein said first input terminal is coupled by ~~a respective conductive~~ said one or more interconnection layers ~~in said layer~~ to a stable voltage signal line.

8. (CANCEL)

9. (CURRENTLY AMENDED) The integrated circuit of claim ~~8~~7, wherein said stable voltage line is a power rail.

10. (CANCEL)

11. (CANCEL)

12. (CURRENTLY AMENDED) The integrated circuit of claim ~~10~~ 1, wherein said ~~used sub-circuit cell~~ reusable circuit cell is configured as a repeater cell in a routing connection across said second area when said reusable circuit cell is coupled to said custom specific layer.

13. (CANCEL)

14. (CANCEL)

15. (CURRENTLY AMENDED) An integrated circuit comprising:

a die having a surface;

a first general purpose area of said die ~~containing~~ comprising general purpose circuit elements configurable by user defined interconnections from above said surface; and

a plurality of second standard circuit areas ~~containing~~ comprising standard sub-circuits having one or more reusable circuit cells more complicated than said general purpose circuit elements and configurable by user defined interconnections from above said surface;

wherein (i) said plurality of second standard circuit areas are distributed across said first general purpose area at multiple locations and (ii) said one or more reusable circuit cells provides functionality that is reusable ~~provide locally usable resources~~ at said multiple locations in said first general purpose area.

16. (ORIGINAL) The integrated circuit of claim 15, wherein said plurality of second standard circuit areas are distributed in a substantially uniform pattern.

17. (ORIGINAL) The integrated circuit of claim 15, wherein said plurality of second standard circuit areas are distributed according to a repeating pattern.

18. (ORIGINAL) The integrated circuit of claim 15, wherein said plurality of second standard circuit areas comprise a plurality of circuit arrays.

19. (ORIGINAL) The integrated circuit of claim 15, wherein said general purpose circuit elements comprise logic circuits.

20. (ORIGINAL) The integrated circuit of claim 15, wherein said general purpose circuit elements comprise one or more logic gates.

21. (ORIGINAL) The integrated circuit of claim 15, wherein said standard sub-circuits comprise logic circuits.

22. (ORIGINAL) The integrated circuit of claim 15, wherein said standard sub-circuits comprise a first buffer array circuit cell.

23. (ORIGINAL) The integrated circuit of claim 22, wherein said first buffer array circuit cell comprises an array of buffer circuits, wherein (i) each buffer circuit comprises an input terminal and an output terminal, and (ii) adjacent buffer circuits are oppositely orientated.

24. (ORIGINAL) The integrated circuit of claim 22 wherein said standard sub-circuits further comprise a second buffer array circuit cell extending in a different physical direction from said first buffer array circuit cell.

25. (CANCEL)

26. (CURRENTLY AMENDED) The integrated circuit of claim ~~25~~24, wherein said ~~general purpose logic circuits~~ standard sub-circuits comprise at least one of~~:~~ an individual buffer~~,~~ a logic gate different from said general purpose circuit elements~~,~~ a multiplexer~~,~~ and a flip flop.

27. (ORIGINAL) The integrated circuit of claim 15, further comprising:

at least one layer of conductive interconnections formed on said surface;

wherein (i) said general purpose circuit elements are coupled to said conductive interconnections in said at least one layer, and (ii) said standard sub-circuits are coupled to said conductive interconnections in said at least one layer.

28. (CURRENTLY AMENDED) A method for designing an integrated circuit element, comprising the steps of:

(a) providing a first area of said integrated circuit element comprising first circuit cells configurable by user defined interconnections above a surface of said integrated circuit element; and

(b) providing a second area of said integrated circuit element comprising a plurality of sub-circuit cells forming a module ~~having a predefined functionality~~, wherein said sub-circuit cells ~~include at least one second circuit cell configured such that when said predefined functionality of said module is not used, said second circuit cell is configurable by user defined interconnections from above said surface~~ includes (i) one or more non-reusable circuit cells coupled to a custom specific layer in a custom design having a predefined functionality and (ii) one or more reusable circuit cells coupled to said custom specific layer in said custom design when said predefined functionality of said module is not used.

29. (NEW) The integrated circuit of claim 1, wherein said custom specific layer comprises one or more interconnection layers.

30. (NEW) The integrated circuit of claim 6, wherein said one or more reusable circuit cells are coupled to said one or more interconnection layers with said first input terminal and said first output terminal.

31. (NEW) The integrated circuit of claim 1, wherein said reusable circuit cell includes one or more buffers and one or more invertors to provide functionality that is reusable.

32. (NEW) The integrated circuit of claim 1, wherein said custom specific layer is positioned above a conductive layer having one or more power distribution lines.

33. (NEW) The integrated circuit of claim 1, wherein said module includes one or more buffer stacks, multi-location memories, signal processor cores, general processor cores, mathematical processor cores, encoders, decoders, transmitters, receivers, communication circuits, analog circuits, and hybrid circuits.

34. (NEW) The integrated circuit of claim 15, wherein said standard sub-circuits comprises one or more non-reusable circuit cells to form one or more modules with one or more reusable circuit cells.

35. (NEW) The integrated circuit of claim 34, further comprising:

a customer specific layer in a custom design coupled to (i) said one or more non-reusable circuit cells in a custom design for said modules with a predefined functionality and (ii) said one or more reusable circuit cells in said custom design when said predefined functionality for said modules is not used.